

FIG. 1

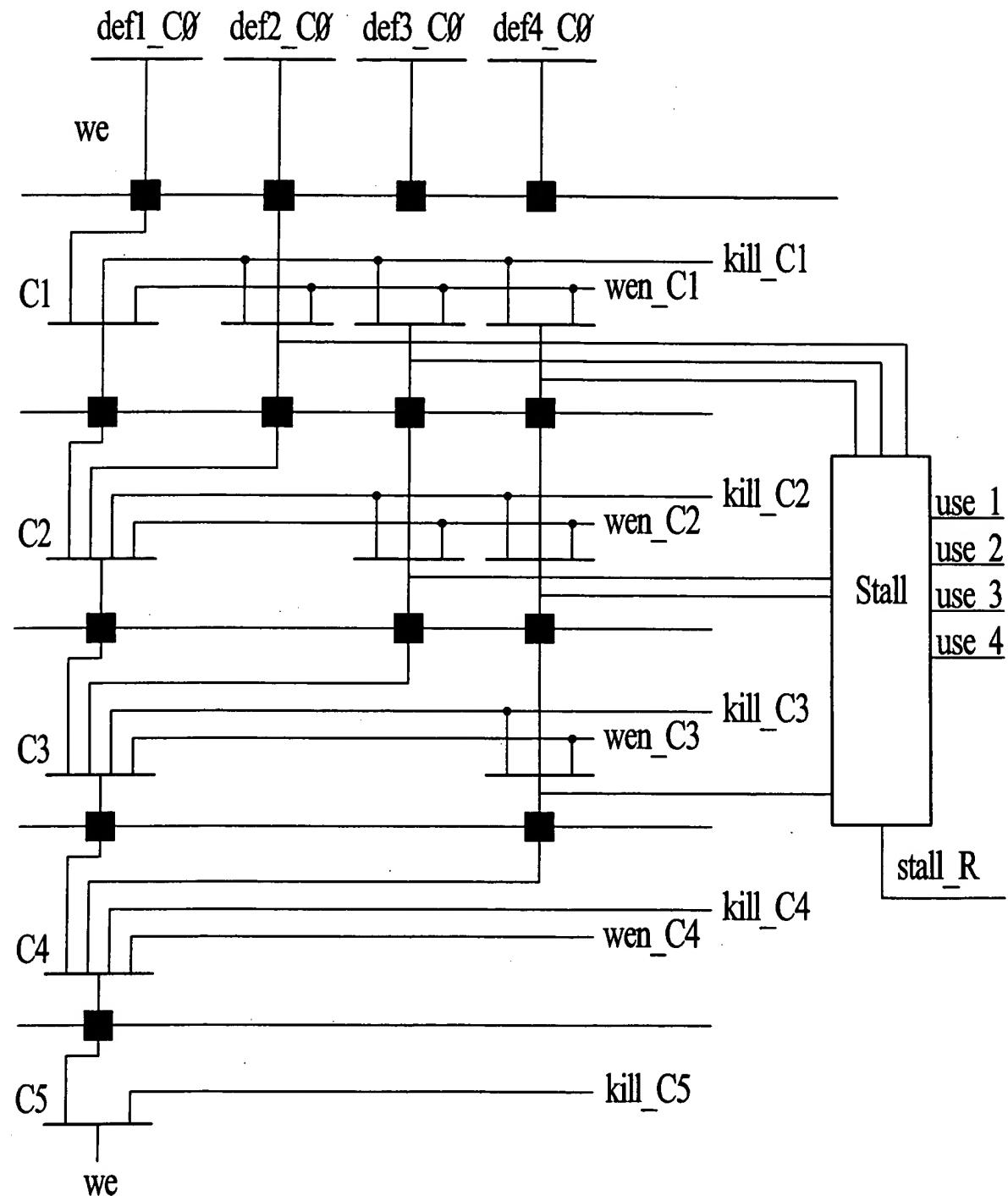
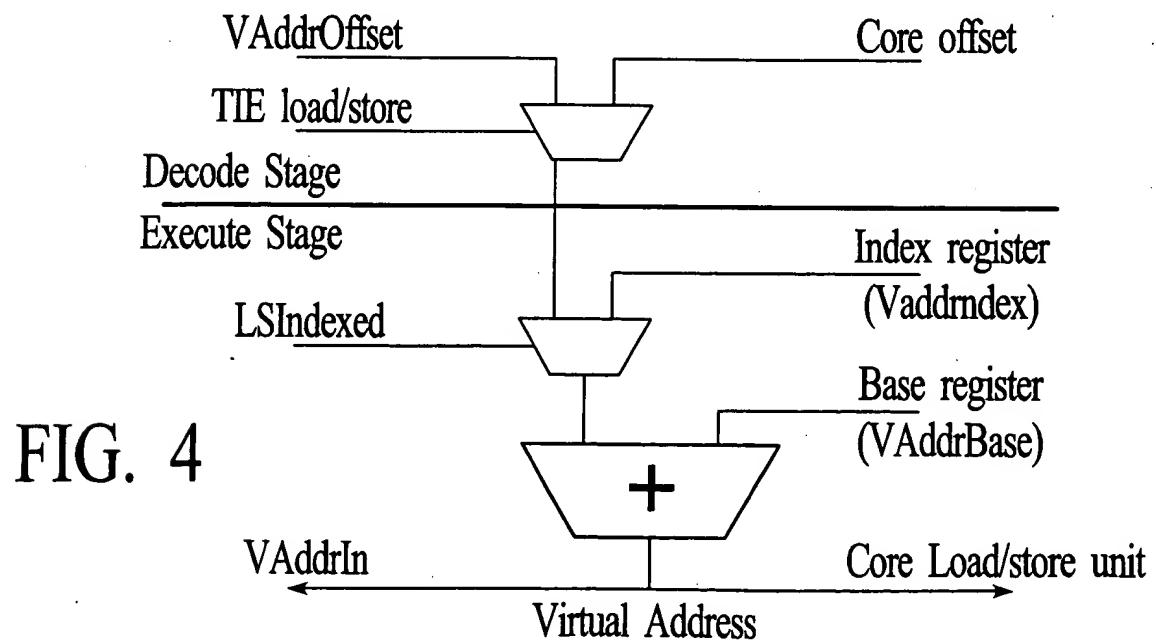
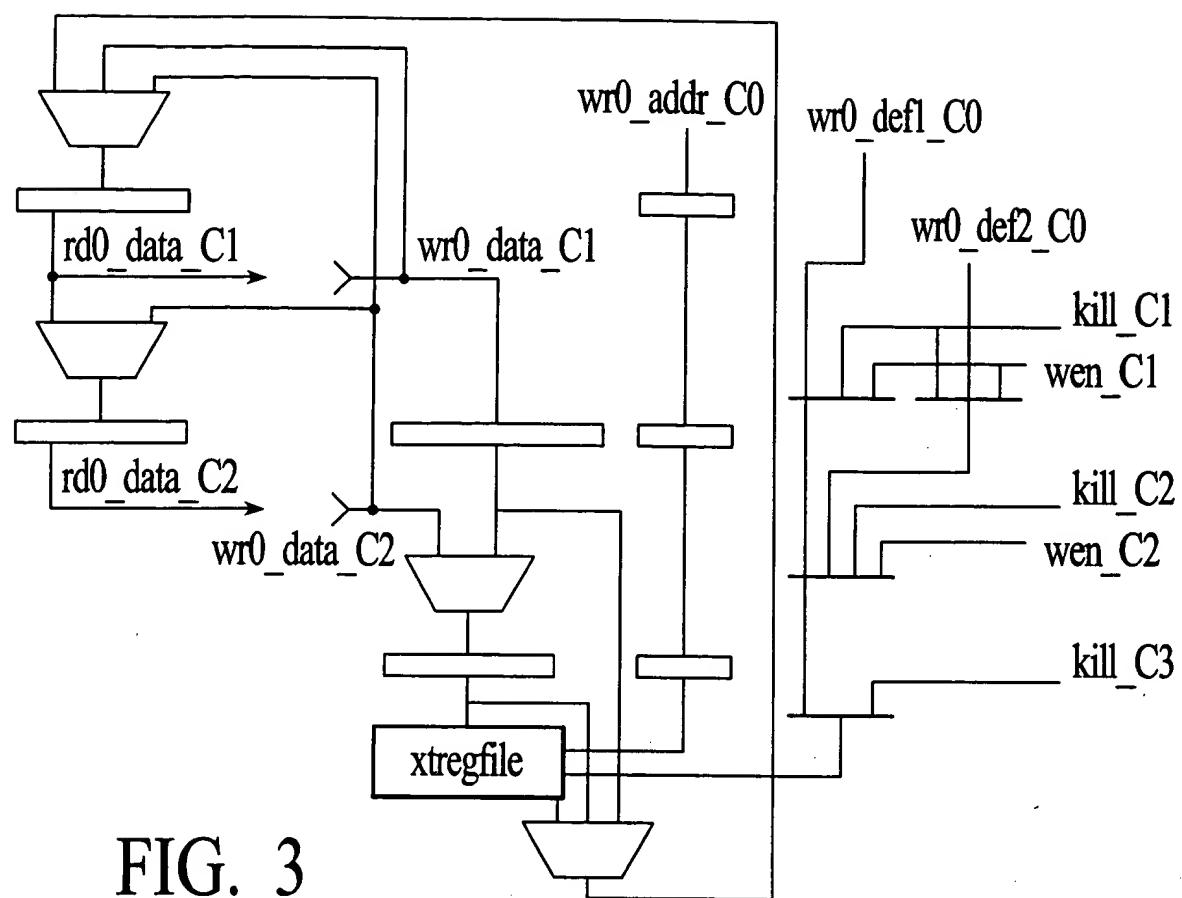


FIG. 2





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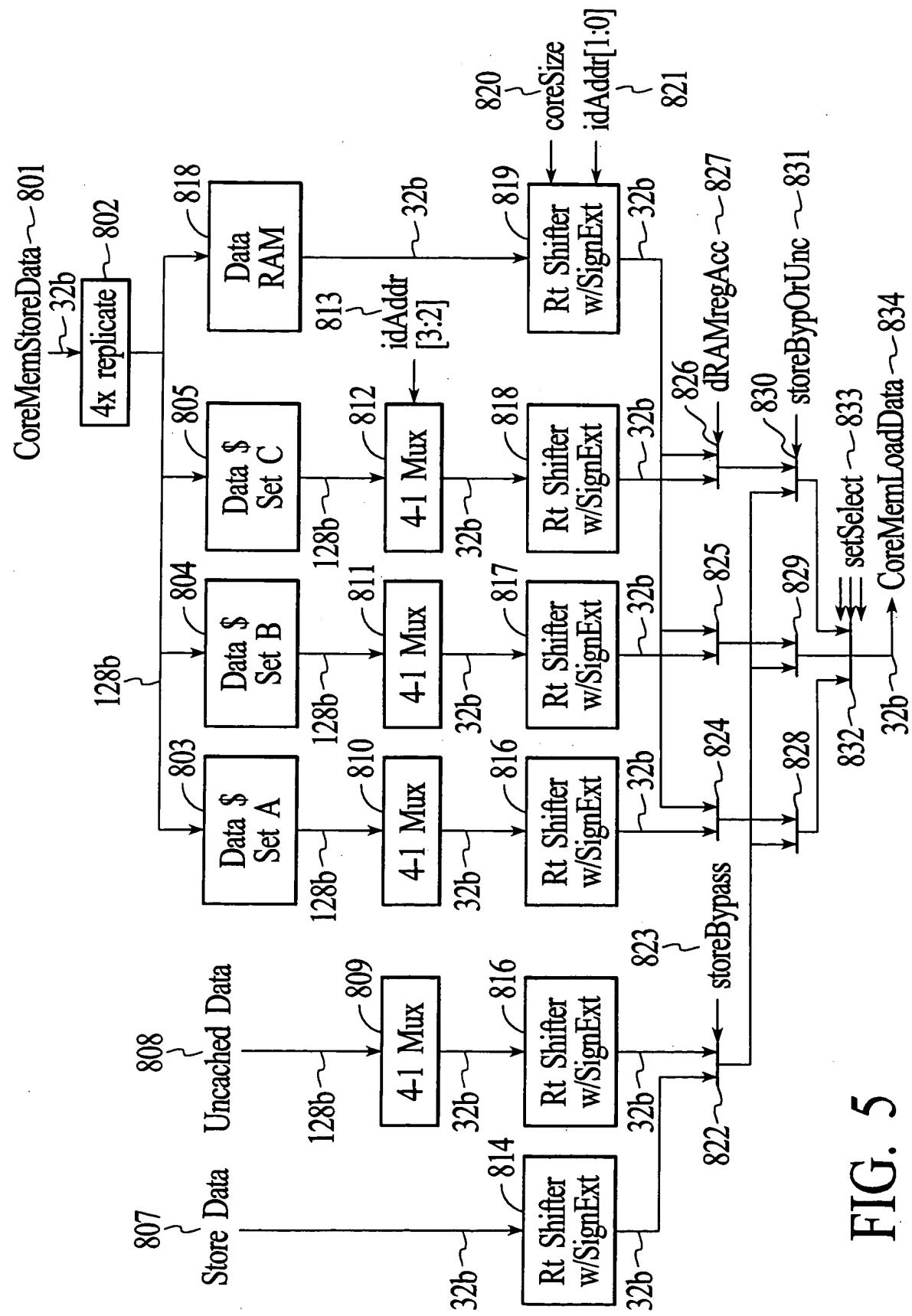
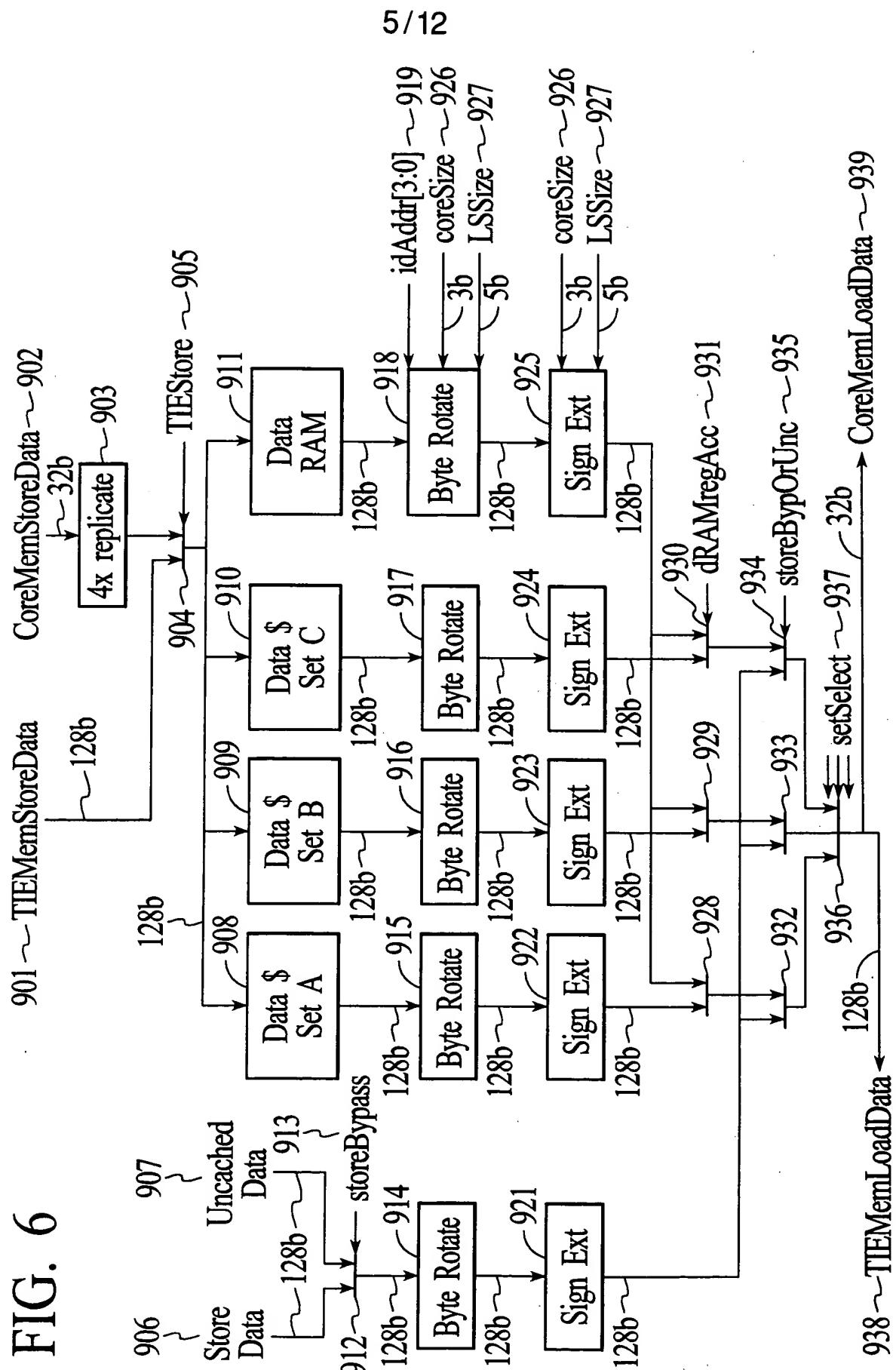


FIG. 5



FIG. 6





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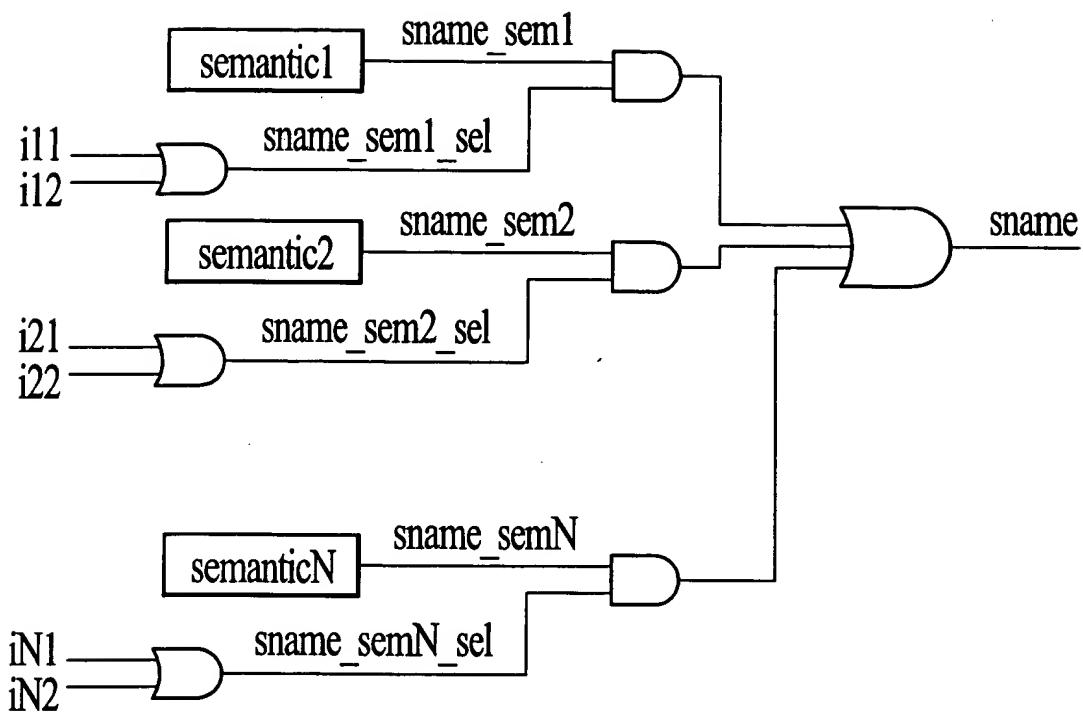


FIG. 7

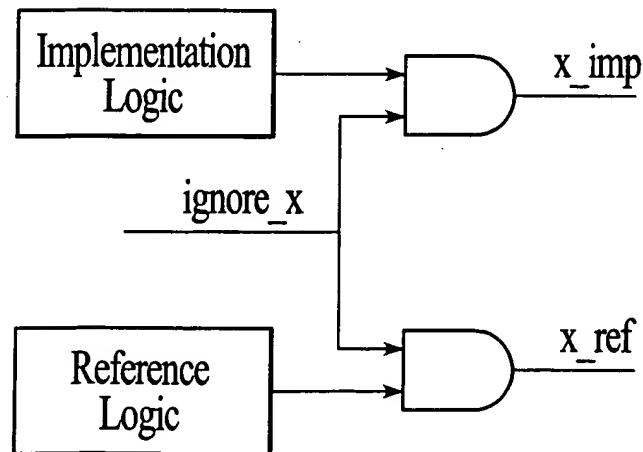


FIG. 11

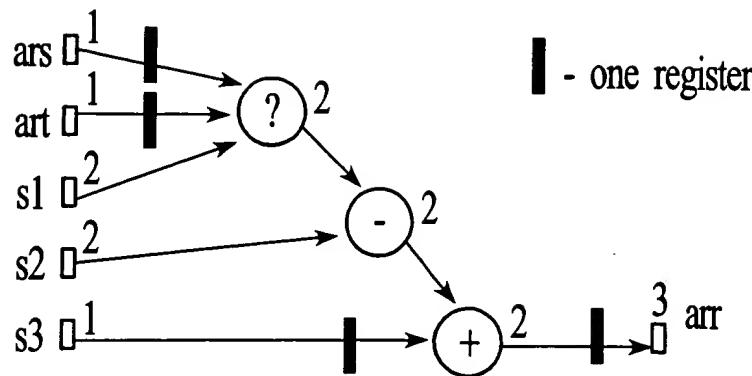


FIG. 8A

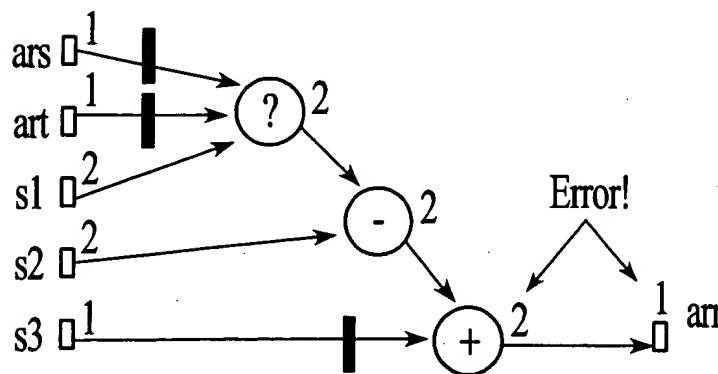


FIG. 8B

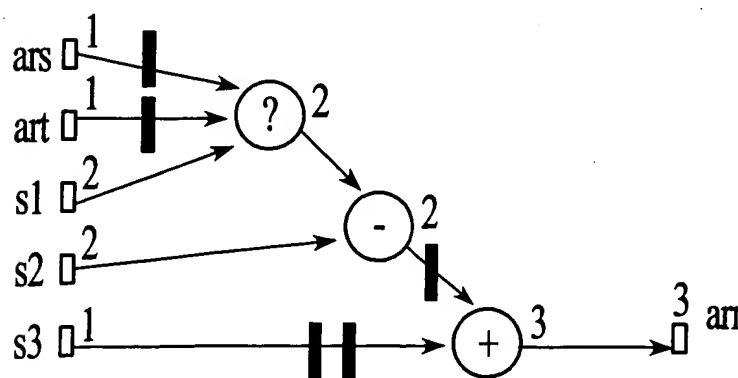


FIG. 8C



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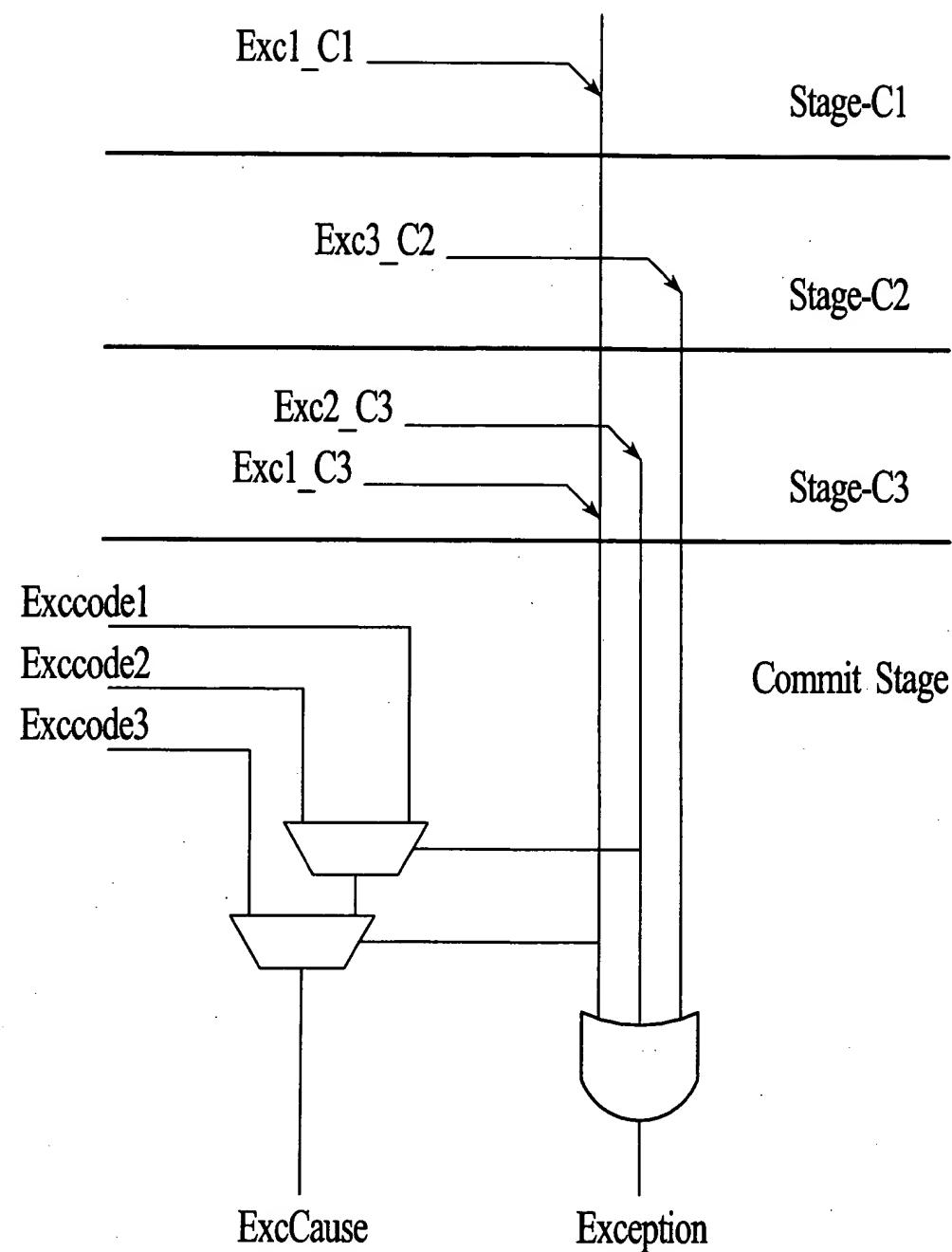


FIG. 9

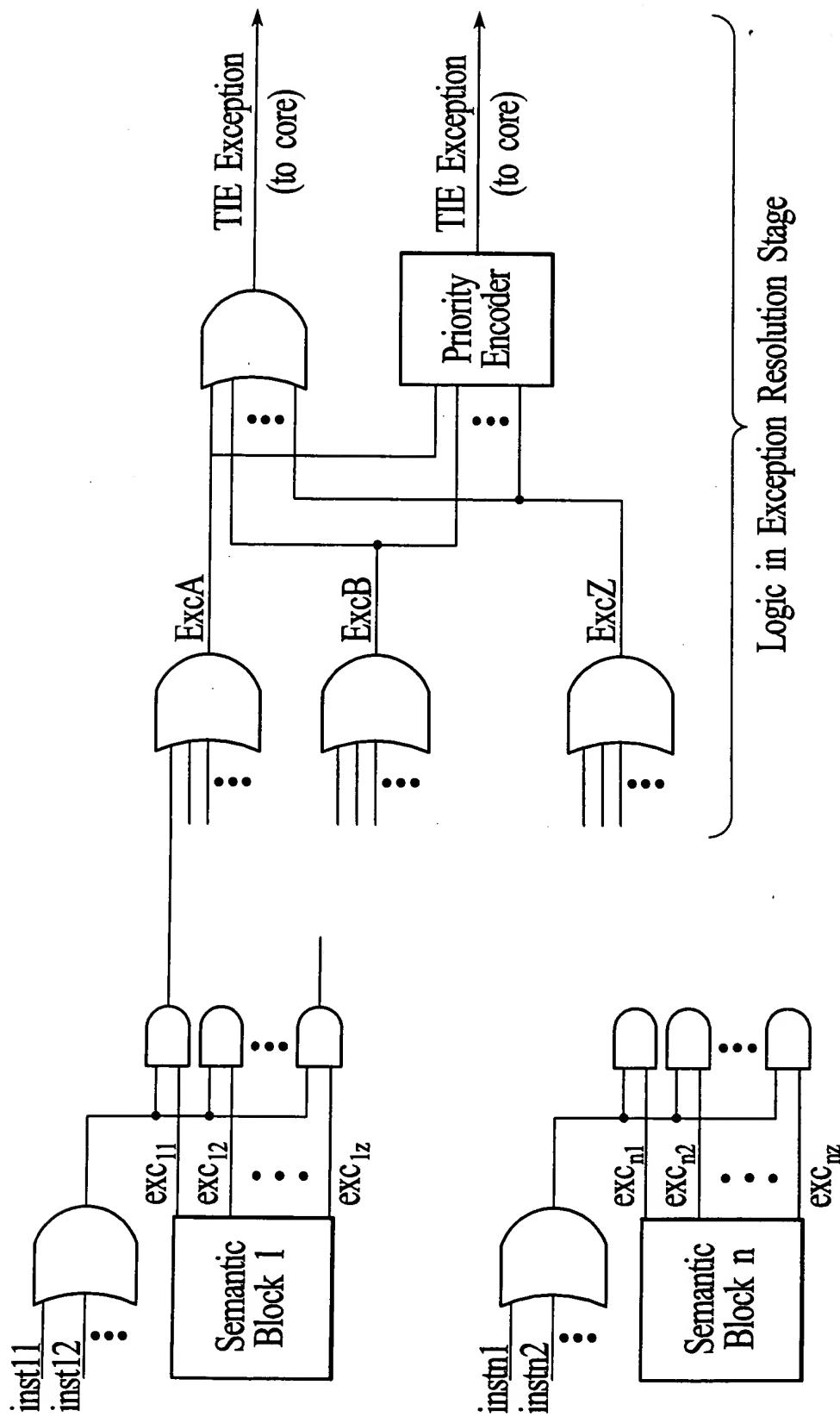


FIG. 10



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MAX40

4 Parallel 40-bit Maximum

Instruction Word

23	16	15	12	11	8	7	4	3	0
0 0 1 1 1 1 0 1		r		s		t		0 0 0 0	
8	4	4	4	4	4	4	4	4	

Package

Vector Integer Coprocessor

Assembler Syntax

MAX40 vr, vs, vt

Description

MAX40 calculates the 40-bit two's complement maximum value for each of the 4 elements of vector registers vs and vt. The result elements are written to vector register vr.

Operation

$$\begin{aligned}
 vr = & \{((\{\sim vs[159], vs[158:120]\}) < (\{\sim vt[159], vt[158:120]\})) ? \\
 & vt[159:120] : vs[159:120], ((\{\sim vs[119], vs[118:80]\}) < (\{\sim vt[119], \\
 & vt[118:80]\})) ? vt[119:80] : vs[119:80], ((\{\sim vs[79], vs[78:40]\}) < \\
 & (\{\sim vt[79], vt[78:40]\})) ? vt[79:40] : vs[79:40], ((\{\sim vs[39], \\
 & vs[38:0]\}) < (\{\sim vt[39], vt[38:0]\})) ? vt[39:0] : vs[39:0];
 \end{aligned}$$

Exceptions

None

FIG. 12

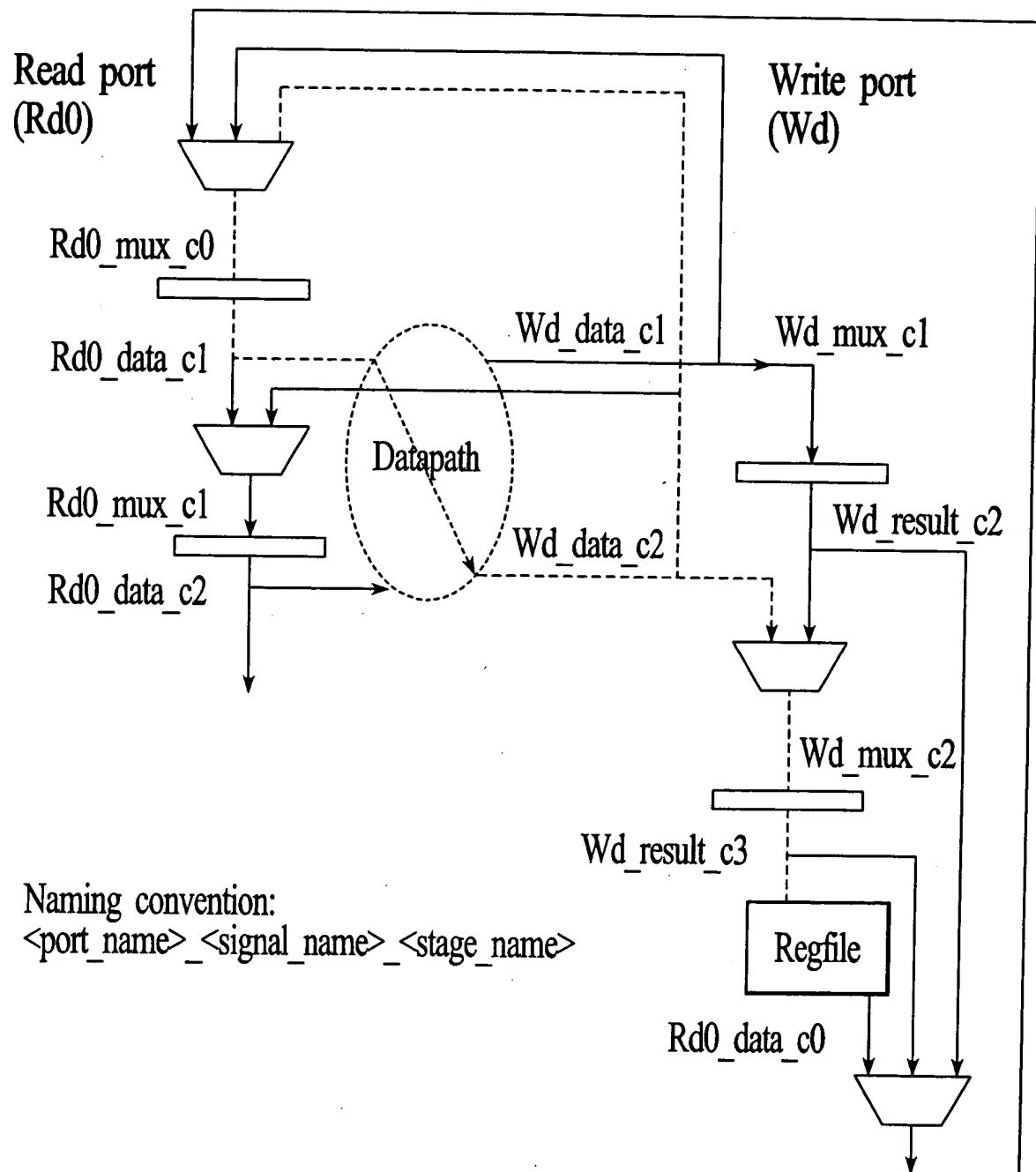


FIG. 13

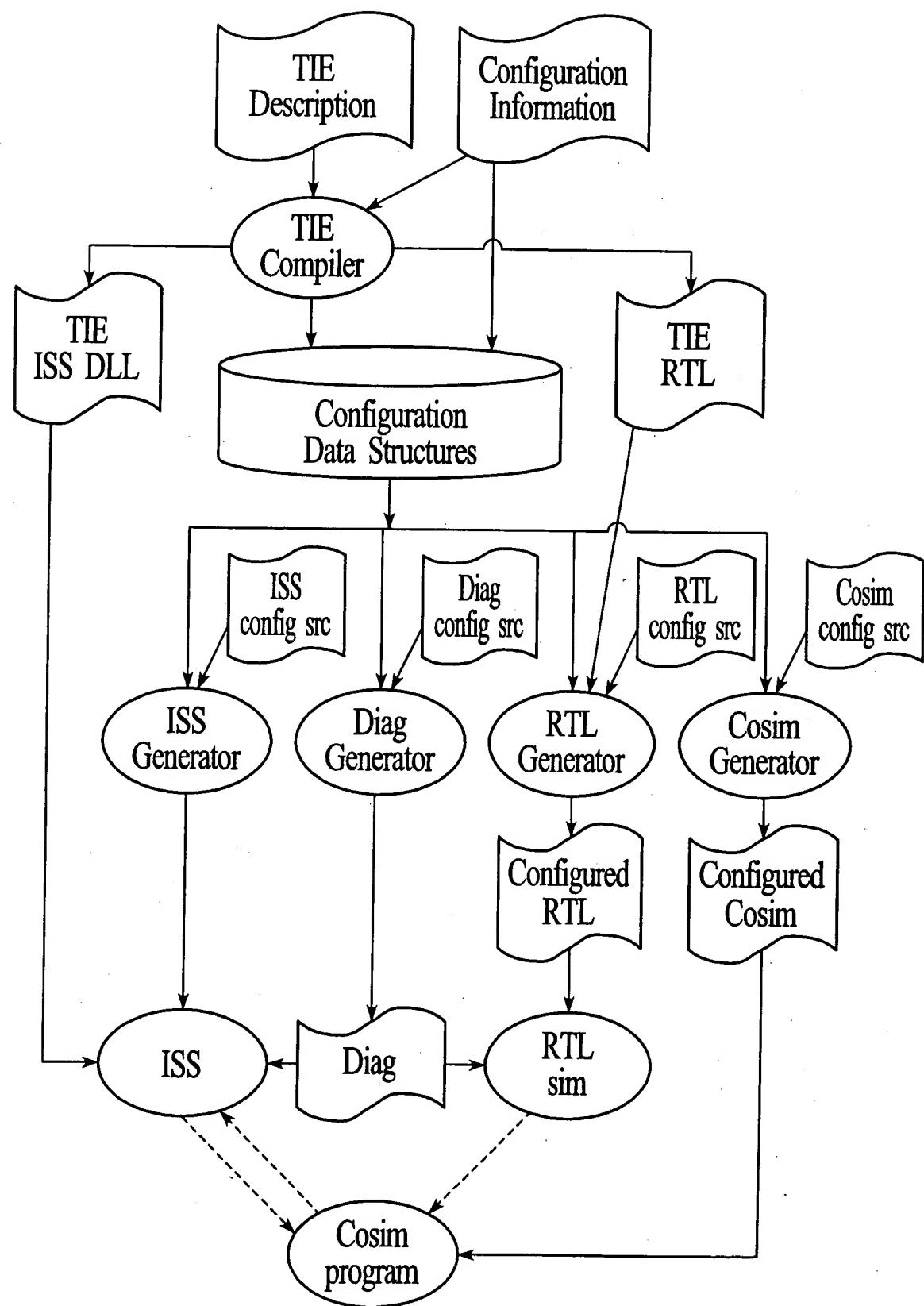


FIG. 14